APPLICATION NOTE

Digital Video Decoder/Encoder Module System: ENCMOD03 + I²C Interfacing

AN97011

Philips
Semiconductors

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Application Note AN97011

Abstract

This application note is intended to provide application support for Philips´ Digital Video Decoders and Encoders. It contains a description of various evaluation boards as well as I²C-bus programming of the ICs.

The Digital Video Decoder converts an analog video input signal into a digital output signal. This signal can be processed by a wide range of applications and fed to the Digital Video Encoder, which delivers analog video signals to TV receivers or video cassette recorders.

This note gives a detailed description of the schematics and some hints how to design the PCB (Printed Circuit Board) with mixed analogue and digital signal processing.

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Digital Video Decoder/Encoder Module System: ENCMOD03 + I²C Interfacing

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Author:

Thomas Grube
Systems Laboratory Hamburg,
Germany

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Summary

This application note is intended to provide application support for Philips´ Digital Video Decoders and Encoders in addition to the application note AN96055. It contains a description of evaluation boards as well as I²C-bus programming of the ICs.

The Digital Video Decoder converts an analog video input signal into a digital output signal. This signal can be processed by a wide range of applications and fed to the Digital Video Encoder, which delivers analog video signals to TV receivers or video cassette recorders.

This note gives a detailed description of the schematics and some hints how to design the PCB (Printed Circuit Board) with mixed analogue and digital signal processing.

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1. Introduction

The Digital Video Decoder/Encoder Modules provide the basis to evaluate various Philips digital video decoders and encoders and give the opportunity to simply insert the modules into customized applications and systems. This application note is an extension to application AN96055 (Digital Video Decoder/Encoder Module System) and contains additional information about the module ENCMOD03 and I²C-bus interfacing (3V/5V level translation).

On the following pages the schematics of the Digital Video Encoder Module ENCMOD03 are shown. The module can be operated in stand alone operation (colourbar generator) as well as extension to other systems like PCI-bridges, MPEG decoders or Video input/output systems.

The module has a socket for an I²C-bus EEPROM (e.g. PCF8582, PCF8594, PCF8598, X24164) in order to store data for initialization and for simple control functionality operated by a (future) microcontroller module. Software for IBM compatible personal computers enables access to all features and settings of the devices. It handles the I²C-bus via a printer port adaptor.

This modular concept was designed to combine different video decoders with various video encoders. Each module can be configured for several devices and packages without the necessity of having a new PCB. This could be achieved by using multiple footprints for one IC and some configurational parts. For interfacing a 26-pin and a 16-pin flat ribbon cable connector is used. The 26-pin YUV-Feature Connector is used for the signal path while the other one is used for power supply and I²C-bus.

2. Digital Video Encoder Module ENCMOD03

The digital encoder module ENCMOD03 contains the encoder SAA7120/21 in QFP44 package. The digital data are accepted in CCIR 656 format (D1). The outputs of the D/A converters are fed through analog postfilters to the connectors.

To allow future ICs to be assembled on this module, some provisions have been done. The filters are assigned to the connectors, so that for each signal type the serial resistor and the filter can be optimized. The signals out of the D/A converters are routed via jumpers to adapt the different output modes of future ICs (JP22, JP23).

RGB signals can be fed to the future encoder via connector J3 . The RGB inputs are connected to the IC via optional resistor dividers to adapt the input voltage range and to terminate the lines.

The clock and synchronization signals can be fed to the encoder via jumper (JP10, JP11, JP15) when operating the slave mode (JP21 open). Using the encoder as clock master (JP21 closed) LLC is supplied by XCLK out of the SAA7120/21. The pins RCV1 and RCV2 can be configured to outputs via I²C-bus setting (see I²C-bus register 6Bh in datasheets) to provide horizontal and vertical synchronization signals.

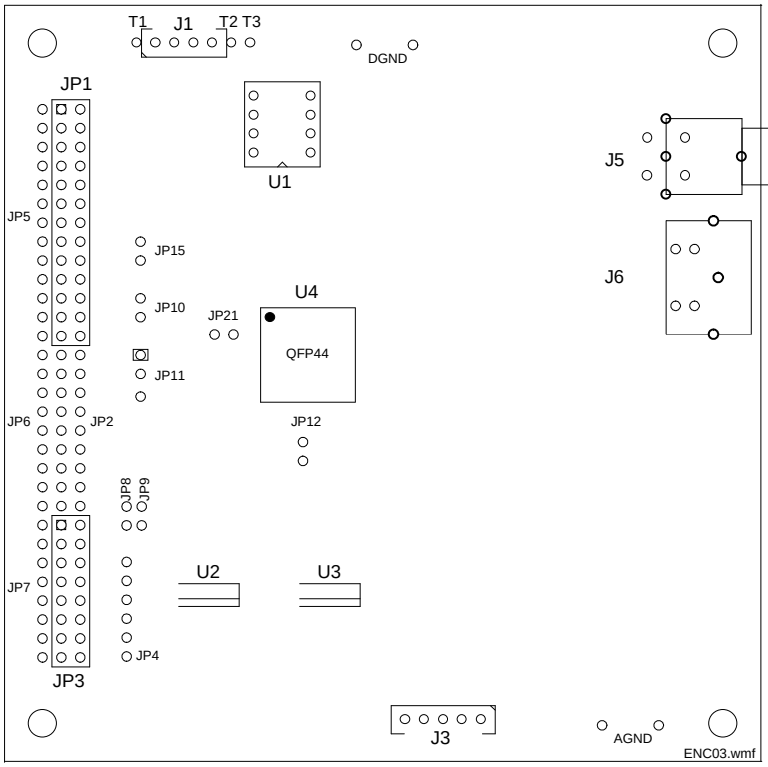


Fig.1 Location of ICs, jumpers and connectors on the ENCMOD03 PCB

TABLE 1 Configuration ENCMOD03

Part	Value	Description
JP12	**closed** open	**slaveaddress 88h** slaveaddress 8Ch
JP8, JP9	**closed**	connection of (5V-) I²C-bus to system connector
R55, R56	0R	**only** stuffed, if **no** 3V to 5V adaption of I²C levels
R53, R54	3k	stuffed for 3V to 5V adaption of I²C levels
Q2, Q3	BS170	stuffed for 3V to 5V adaption of I²C levels
R35	0R	connection AGND to DGND near encoder
R34	open	termination LLC
JP15	**closed**	jumper LLC (clock from/to feature connector)
JP21	closed **open**	connects the XCLK output with the LLC input
JP11		HS/HREF to/from RCV2
JP10		VS to/from RCV1
J3	RGBin	RGB input connector (for future ICs) R15,16,17,18,23,24,26,27 used to adapt input voltage range
T5	RESN	testpin (active low reset input)
T7	TTXRQ	testpin (output signal for teletext request)
T8	TTX	testpin (input signal for teletext data)
R62, R63	0R	connection of TTX and TTXRQ to system connector
JP19		to be stuffed for future ICs
JP20		to be stuffed for future ICs
JP22		to be stuffed for future ICs
JP23		to be stuffed for future ICs
R57, R59	0R	to be left open for future ICs
R58, R60, R61	open	to be stuffed 0R for future ICs
R64, R65, R66	0R	to be left open for future ICs
JP2		additional pins for using a 60 pin header for JP1, JP2 and JP3
JP4		additional testpins connected to reserved pins on JP3
JP5 JP6 JP7		additional pins for using reverse connectors

Remark:

The parts mentioned in Table 1 are only for evaluation purpose and can be omitted in an application.

3. I²C-bus EEPROM on DECMOD01, ENCMOD02 and ENCMOD03

The IC U1 on each module can be assembled with different IC types depending on the desired memory size. Additionally the I²C-bus device address can be adapted by soldering corresponding SMD resistors which is described in the tables below.

TABLE 2 Configuration of I²C-bus EEPROMs

IC type	Size	Pin 1	Pin 2	Pin 3	Pin 7	Address Range
PCF8582x-2	256 bytes	**A0:** "0" "1" "0" "1" "0" "1" "0" "1"	**A1:** "0" "0" "1" "1" "0" "0" "1" "1"	**A2:** "0" "0" "0" "0" "1" "1" "1" "1"	PTC	A0h **or** A2h **or** A4h **or** A6h **or** A8h **or** AAh **or** ACh **or** AEh
PCF8594x-2	512 bytes	WP	**A1:** "0" "1" "0" "1"	**A2:** "0" "0" "1" "1"	PTC	A0h and A2h **or** A4h and A6h **or** A8h and AAh **or** ACh and AhE
PCF8598x-2	1024 bytes	WP	n.c.	**A2:** "0" "1"	PTC	A0h, A2h, A4h and A6h **or** A8h, AAh, ACh and AEh
X24164	2048 bytes	**S0:** "0" "1" "0" "1" "0" "1" "0" "1"	**S1:** "1" "1" "0" "0" "1" "1" "0" "0"	**S2:** "0" "0" "0" "0" "1" "1" "1" "1"	TEST	80h, 82h, 84h, 86h, 88h, 8Ah, 8Ch and 8Eh **or** 90h, 92h, 94h, 96h, 98h, 9Ah, 9Ch and 9Eh **or** A0h, A2h, A4h, A6h, A8h, AAh, ACh and AEh **or** B0h, B2h, B4h, B6h, B8h, BAh, BCh and BEh **or** C0h, C2h, C4h, C6h, C8h, CAh, CCh and CEh **or** D0h, D2h, D4h, D6h, D8h, DAh, DCh and DEh **or** E0h, E2h, E4h, E6h, E8h, EAh, ECh and EEh **or** F0h, F2h, F4h, F6h, F8h, FAh, FCh and FEh

TABLE 3 Board Configuration for I²C-bus EEPROMs

Pin	"0"	"1"	Remark
PTC or TEST	R4: OPEN R8: 0R	R4: 0R R8: OPEN	Leave pin PTC open; apply "0" to pin TEST
A2 or S2	R5: OPEN R9: 0R	R5: 0R R9: OPEN	
A1 or S1	R6: OPEN R10: 0R	R6: 0R R10: OPEN	pin S1 (X24164) is inverted internally
WP, A0 or S0	R7: OPEN R11: 0R	R7: 0R R11: OPEN	WP: "1" --> write protect of upper 256[512] bytes "0" --> write enabled (only PCF8594[PCF8598])

Note: The modules will be stuffed by default using the following slaveaddresses (8-bit notation):

EEPROM - type:	Decoder Modules:	Encoder Modules:
PCF8582x-2	A6h	A8h
PCF8594x-2:	A4h, A6h, WP=1	A8h, AAh, WP=0
PCF8598x-2:	A0h, A2h, A4h, A6h, WP=1	A8h, AAh, ACh, AEh, WP=0
X24164:	90h, 92h, 94h, 96h, 98h, 9Ah, 9Ch and 9Eh	E0h, E2h, E4h, E6h, E8h, EAh, ECh and EEh

4. Module System Connectors

The YUV connector (feature connector) provides access to the digital YUV data input coming from a digital video decoder or from an MPEG video source supplied to a video encoder. Two YUV data formats are supported, 16-bit “decoder format” or 8-bit CCIR656 compatible (D1). The control lines are set either as inputs or outputs. The connector has the following pin assignment:

Pin 1, 3, 5, 7, 9, 11, 13, 15	UV0: UV7 digital UV data (not used on ENCMOD03)
Pin 2, 4, 6, 8, 10, 12, 14, 16	Y0: Y7 digital CCIR656 data
Pin 17	LLC digital clock
Pin 18	LLC2 (not used on ENCMOD03)
Pin 19	CREF, clock reference (not used on ENCMOD03)
Pin 20	HREF, optional horizontal reference (blanking)
Pin 21	RTC, real time control
Pin 22	HS, horizontal synchronisation pulse
Pin 23	digital ground
Pin 24	VS, vertical synchronisation pulse
Pin 25	DIR
Pin 26	digital ground

The 16-pin header for power supply and I²C-bus has the following pin assignment:

Pin 1	SCL
Pin 2	SDA
Pin 3, 9, 15, 16	reserved for future use
Pin 4	TTXRQ (teletext data request output from encoder)
Pin 5, 6	digital power supply (5V)
Pin 7, 8	digital groundl
Pin 10	TTX (teletext data input to encoder)
Pin 11, 12	analog power supply (12V)
Pin 13, 14	analog ground

On each module in addition (or as alternative) a 4 pin connector can be used for I²C-bus control:

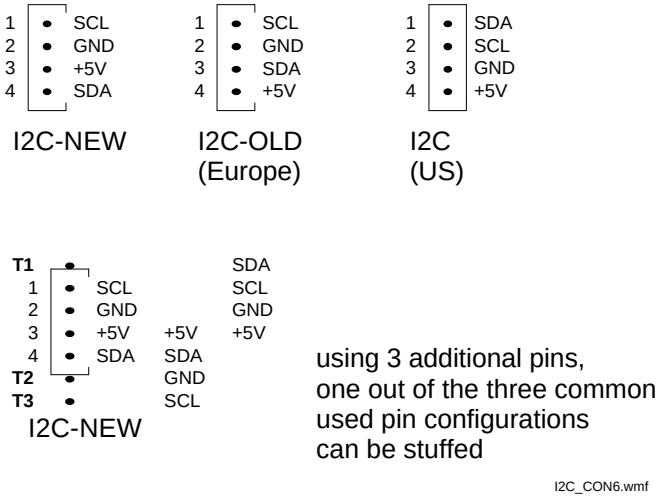


Fig.2 I²C-bus connector pinnings

Note: Always supply the I²C-bus with pull-up resistors, but avoid too high currents (see I²C-bus specification). On each module pull-up resistors can be added (R1 and R2), but preferably only one pull-up should be done on the I²C-bus master IC.

5. I²C-Bus Interface H6ACS38

For systems running in a 3.3V environment it is required to use an I²C-bus interface with 3.3V capability. The new Single Master Interface H6ACS38 with the IC 74HC9114D replaces former Single Master Interfaces with the IC 74LS05 (e.g. H3VS15), which is only suited for 5V. The new interface operates on the I²C-bus from 1.8V to 5V.

The 74HC9114 is a nine wide Schmitt-Trigger buffer with open drain inverting outputs, which are not clamped by diodes connected to V_{CC}. This allows the device the operation as level shifter with the output to be pulled between GND and V_{Omax}. There are three options to represent (or to support the internal) pull-up resistors at the input lines of the PC´s parallel port (see also schematics of H6ACS38 in appendix):

1.) the databits at portpins 2 ~ 4 of the LPT connector (D-SUB25) are connected via 10k resistors R1 ~ R3 to pins 11, 12 and 15 (input lines)
2.) if VDD on the I²C-bus connector is high enough, the resistors R7 ~ R9 get the supply via diodes D4 ~ D6
3.) an external supply can be fed to R7 ~ R9 via diodes D1 ~ D3

The pull-up resistors on the interface to the PC side are supplied by unused databits which should be programmed to “1” by the I²C-bus driver software. Together with the LPT-internal pull-ups this should operate. Due to the various different implementations of parallel port interfaces (LPT) in Personal Computers in a few cases it could be required to add an additional supply voltage of 5V to the interface to meet the correct input levels. Therefor two pads are foreseen on the interface PCB (named “+5V” and “GND”).

If the databits are set to “0”, R1 ~ R3 act as load and decrease the signals. If no external 5V supply is available, it is then possible to remove R1 ~ R3. In that case, the LPT portpins must have their own pull-ups.

The I²C-bus driver ´Í2CDRV.DLL´ (96-03-22 10:46, 52192 byte; supplied with the Universal Register Debugger software) switches the databits to “0” during a start condition, but this does not influence the I²C transmission. The driver ´I2CAPI.DLL version 1.0.0.3´ (supplied with several tools from the Systems Laboratory Hamburg) tests in addition the performance of the LPT-port signals. If the low to high transition is too slow (more than 1µs), the interface detection will fail. This can be caused by too high ohmic pull-up resistors or too much capacitive load due to long interface cables (e.g. 25 pin flat ribbon cable). In some configurations (e.g. PC-Laptop with capacitors at LPT-portpins; Error message: ´No I2C device on parallel port´) two additional pull-up resistors (1...4k7) should be added to the input pins 1 and 3 of the 74HC9114. They can be either connected to VCC or to another unused portpins (like R1~R3 and R7~R9; e.g. use with pins 5~8 of SUB-D 25pin connector).

The DTV (MPC-E) debugger software (versions 1.0x) does not affect the databits, so that they remain in their prior state. This can cause problems when the I²C-bus supply is less than 5V and the bits are “0” (workaround: see above).

The software IICTV (and related DOS based software packages from Philips Semiconductors) set the databits to “1” so that no problems are expected with R1~R3.

The lower the supply voltage of the I²C-bus the lower the pull-up resistors have to be, to ensure a specific current. Additionally noise margins get smaller and voltage drops over serial resistor become more important. These things have to be considered for designs with low voltage I²C-bus.

6. I²C-Bus Level Shifter

On the Encoder Module ENCMOD03 a circuit was implemented to allow the connection of the internal 3.3V I²C-bus to an external 5V I²C-bus connected via the 16pin system connector (the external I²C-bus has to provide its own pull-up resistors). The circuit also operates with 3.3V levels on the system connector, but if no level conversion is necessary, the circuit can be removed (R53, R54, Q2, Q3) and bypassed with resistors R55 and R56.

The N-channel enhancement mode vertical D-MOS transistors Q2 and Q3 allow the bi-directional I²C-bus operation while shifting the levels. If the bus lines are pulled high (e.g. I²C-bus is inactive) the transistor is in high ohmic state (V_{GS} ~ 0V). If the Source is pulled to GND (3.3V side), V_{GS} exceeds $V_{GS(th)}$ and the transistor conducts so that the Drain is also forced to the level of the Source (low). If the Drain is pulled to GND, the parasitic diode conducts and the Source is also pulled down.

The lower the voltage on the I²C-bus, the more important is the threshold voltage $V_{GS(th)}$ of the transistor. For 3.3V environment, several types can be used (e.g. BSS123 in SOT123 envelope on ENCMOD03). For lower voltages it is recommended to use e.g. BSS138 (SOT123) or BS108 (TO92).

7. Programming tables for SAA7120/21 and SAA7111A

The data tables below show the programming for the SAA7120/21 for operation with SAA7111A (e.g. DECMOD01 connected to ENCMOD03)

SAA7120/21:
- init data
PAL

Slave:	88h
Sub	Data
REG 3a =	13 (93)
REG 5a =	77
REG 5b =	7d
REG 5c =	af
REG 5d =	23 (a3)
REG 5e =	35
REG 5f =	35
REG 60 =	00
REG 61 =	06
REG 62 =	2f (af)
REG 63 =	cb
REG 64 =	8a
REG 65 =	09
REG 66 =	2a
REG 67 =	00
REG 68 =	00
REG 69 =	00
REG 6a =	00
REG 6b =	20
REG 6c =	01
REG 6d =	30
REG 6e =	a0
REG 6f =	00
REG 70 =	00
REG 71 =	00
REG 72 =	00
REG 73 =	00
REG 74 =	00
REG 75 =	00
REG 76 =	00
REG 77 =	00
REG 78 =	00
REG 79 =	00
REG 7a =	00
REG 7b =	00
REG 7c =	00
REG 7d =	00
REG 7e =	00
REG 7f =	00

I2C1120d.mem

SAA7120/21:
- init data
NTSC

Slave:	88h
Sub	Data
REG 3a =	13 (93)
REG 5a =	77
REG 5b =	76
REG 5c =	a5
REG 5d =	2a (aa)
REG 5e =	2e
REG 5f =	2e
REG 60 =	00
REG 61 =	15
REG 62 =	3f (bf)
REG 63 =	1f
REG 64 =	7c
REG 65 =	f0
REG 66 =	21
REG 67 =	00
REG 68 =	00
REG 69 =	00
REG 6a =	00
REG 6b =	20
REG 6c =	11
REG 6d =	31
REG 6e =	80
REG 6f =	00
REG 70 =	00
REG 71 =	00
REG 72 =	00
REG 73 =	00
REG 74 =	00
REG 75 =	00
REG 76 =	00
REG 77 =	00
REG 78 =	00
REG 79 =	00
REG 7a =	00
REG 7b =	00
REG 7c =	00
REG 7d =	00
REG 7e =	00
REG 7f =	00

I2C1120d.mem

SAA7111A:
- init data

Slave:	48h
Sub	Data
00h	00h
01h	00h
02h	D0h (D5h)
03h	00h
04h	00h
05h	00h
06h	F9h
07h	E9h
08h	A8h (2Eh,6Eh)
09h	00h (80h)
0Ah	80h
0Bh	47h
0Ch	40h
0Dh	00h
0Eh	00h
0Fh	00h
10h	D0h
11h	0Ch
12h	01h
1Fh	87h

I2C1120d.mem

Values in brackets:
register 02h: select S-Video input
register 08h: H-PLL opened (50Hz/60Hz forced)
register 09h: Luma bypass for enhanced S-Video performance

Values in brackets:
register 3Ah: Colourbar on
register 5Dh: only use with revision SAA7120/21 V0
register 62h: Real Time Control (RTCE) enabled

INITeI2C.wmf
7120 07.02.96

8. Universal Register Debugger Software

You can install the Universal Register Debugger Software by simply running the SETUP.EXE on the floppy disk. Afterwards you should copy the subdirectory \URDDATA from floppy disk to harddisk. The file \URD-DATA\11A20TG1.URD contains startup information (and a few macros) for the SAA7111A (EVIP) and SAA7120 (CONDENC). The I²C-bus Single Master Interface has to be connected to a printer port and to the Decoder/ Encoder Modules. After powering up the hardware and calling the software, the CVBS2 input (J3, DECMOD01) accepts PAL-B/G input signals to be encoded on the ENCMOD03. The following macros can be used (Macro / Do Macro):

VIP S-Video in:	selects input S-Video (J5) of DECMOD01 (AI12, AI22 of SAA7111A)
VIP CVBS2 in:	selects input CVBS2 (J3) of DECMOD01 (AI11 of SAA7111A)
7120 NTSC:	SAA7120 setup for NTSC-M
7120 PAL:	SAA7120 setup for PAL-B/G
CB PAL:	enables Colourbar Generator Mode of SAA7120; opens H-PLL of SAA7111A and forces 50Hz Note: only use this macro in conjunction with 7120 PAL macro
CB NTSC:	enables Colourbar Generator Mode of SAA7120; opens H-PLL of SAA7111A and forces 60Hz Note: only use this macro in conjunction with 7120 NTSC macro
CB off:	switches colourbar off; closes H-PLL again

On a slow PC it might take a few seconds to run the macros (~10s for 7120 PAL/NTSC on a 386DX33).

The Universal Register Debugger (URD.EXE dated 96-11-06) is a β-release. After starting the software it might be required to enlarge the window in horizontal direction to view and edit the values of the registers.

The URD-files on the disk do not claim to be perfect. Please check with latest datasheet. The file 11A20TG1.URD contains modified settings for SAA7120V0.

9. Tips for a PCB layout with analog and digital signal processing

- use separate ground planes for analog and digital supply in <u>one</u> layer (no overlapping!)
- use separate supply planes for analog and digital with the same shape (or smaller) as ground (no overlap of analog supply with digital ground and vice versa!)
- if there are different (asynchronous) clock domains, use separate ground and supply planes (place the analog areas not in a direct neighbourhood; separate the clock domains)
- always use the inner layers for ground and supply planes (no signal layer in between!)
- try to keep digital signals away from analog areas
- place analog areas close to the border of a PCB
- avoid long tracks for analog signals
- place decoupling capacitors (22nF to 100nF) close to the power pins of the ICs
- prepare several provisions for connecting places for analog and digital ground on the PCB for further optimization on the final board

10. PCB Revisions

	Version	Package	Device(s)	Remarks
DECMOD01:				
	A1:	PLCC68	SAA7110(A)	PLCC socket stuffed; 26.800 MHz crystal
	A2:	PLCC68	SAA7111	PLCC socket stuffed; 24.576 MHz crystal
	A3:	LQFP64	SAA7111A	24.576 MHz crystal
ENCMOD02:				
	A1:	PLCC84	SAA7124/25/82/83	PLCC socket stuffed
	A2:	QFP80	SAA7124	
	A3:	QFP80	SAA7125	
	A4:	LQFP64	SAA7124	
	A5:	LQFP64	SAA7125	
	A6:	PLCC84	SAA7182A/83A	PLCC socket stuffed
	A7:	QFP80	SAA7182A	
	A8:	QFP80	SAA7183A	
ENCMOD03:				
	A1:	QFP44	SAA7120	I²C-bus level shifter 3V/5V stuffed
	A2:	QFP44	SAA7120	I²C-bus 3.3V levels

Note:

- ENCMOD02 Vers. A1~A8 should be combined with DECMOD01 Vers. A2 (5V I/O)
- ENCMOD03 should be combined with DECMOD01 Vers. A3 (3.3V I/O)
- ENCMOD03 and DECMOD01 Vers. A3 (3.3V I/O) should be used with I2C Single Master Interface H6ACS38
- all Encoder Modules require a 27.000 MHz 3rd overtone crystal (only for master mode)

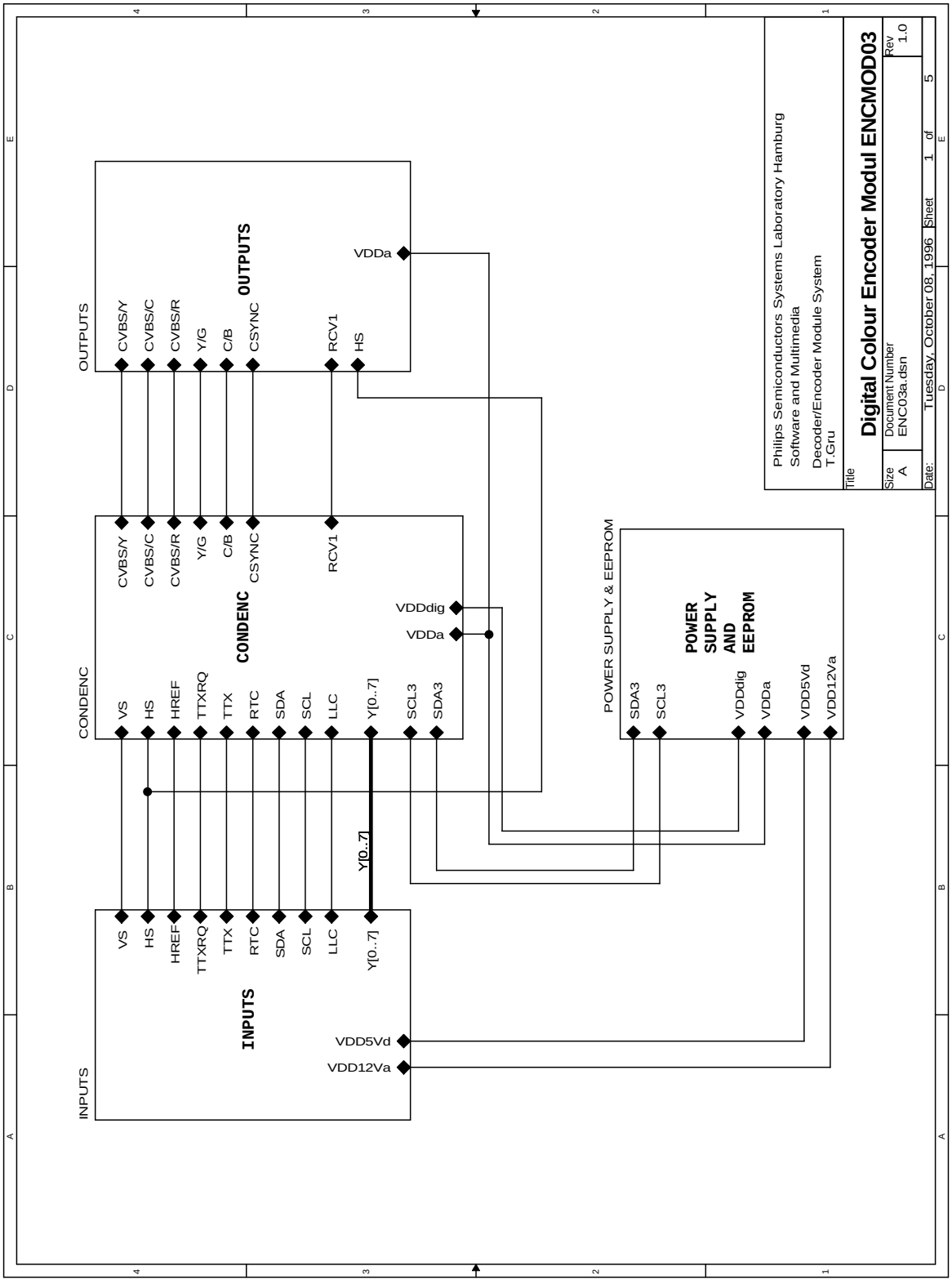
11. Appendix: Schematics and Layout

The schematics are made in OrCAD and the files can be delivered on request.

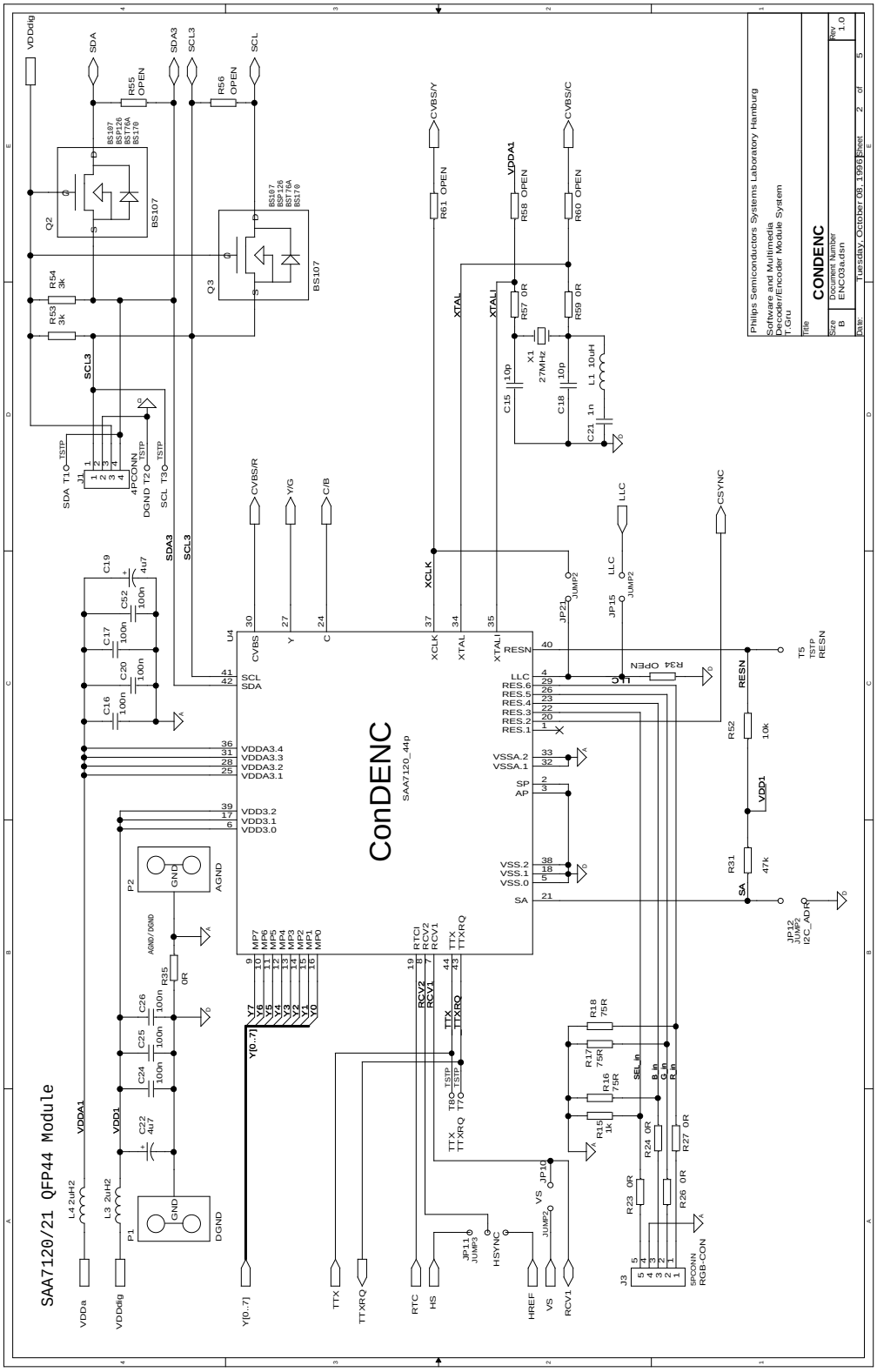
For the board layout GERBER files are available.

11.1 Schematics

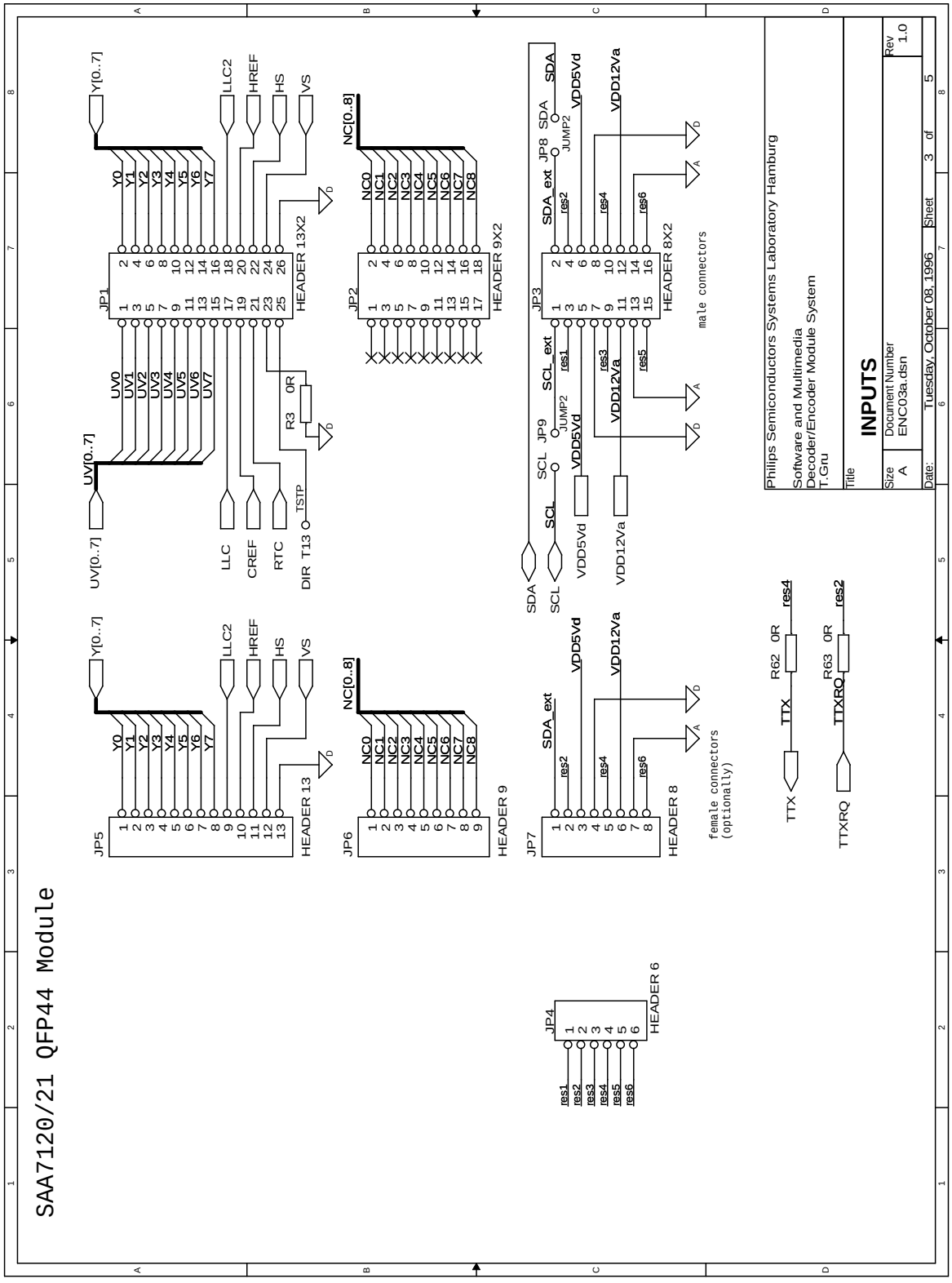
11.1.1 Top sheet of ENCMOD03



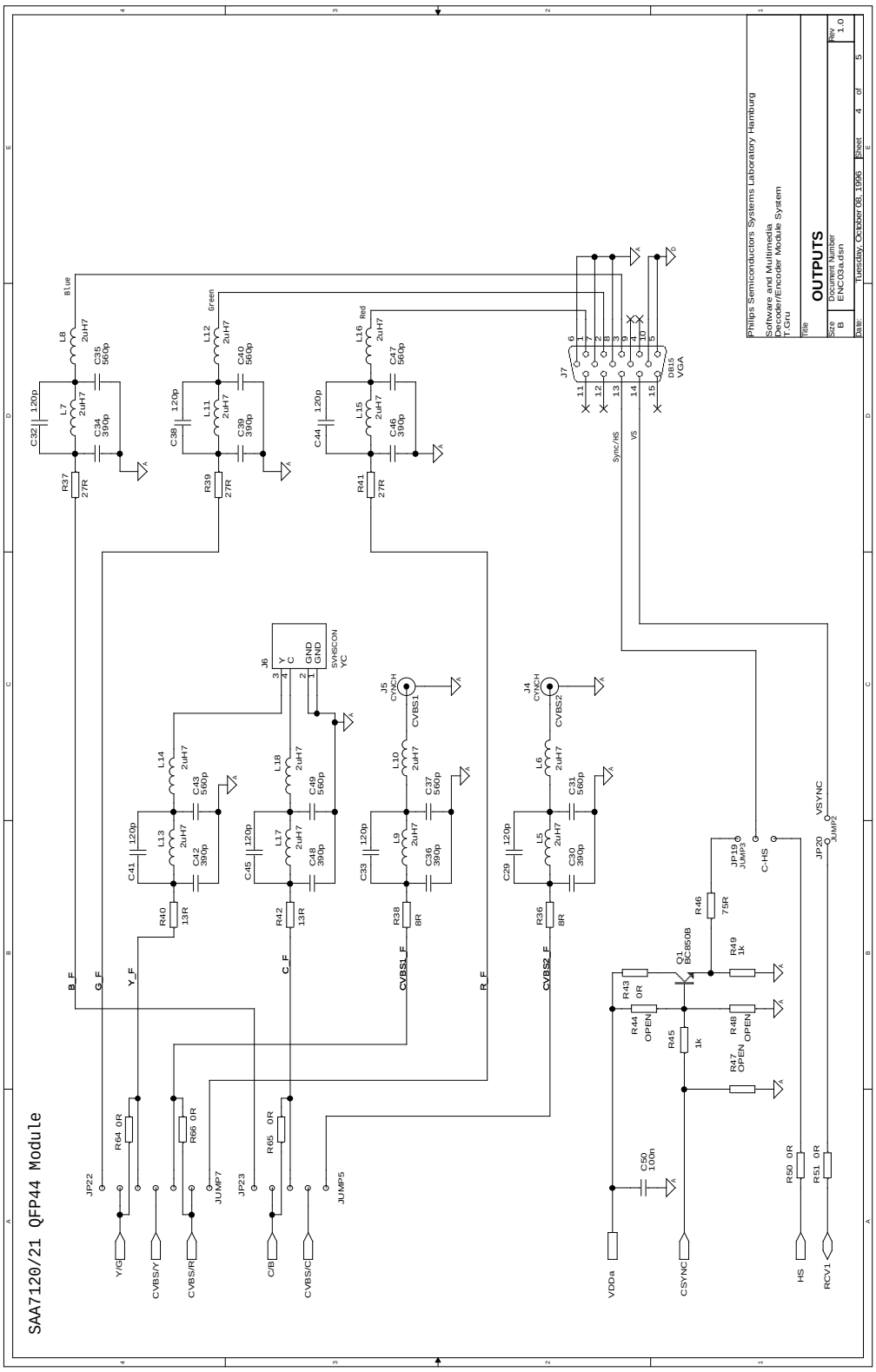
11.1.2 Digital Video Encoder of ENCMOD03



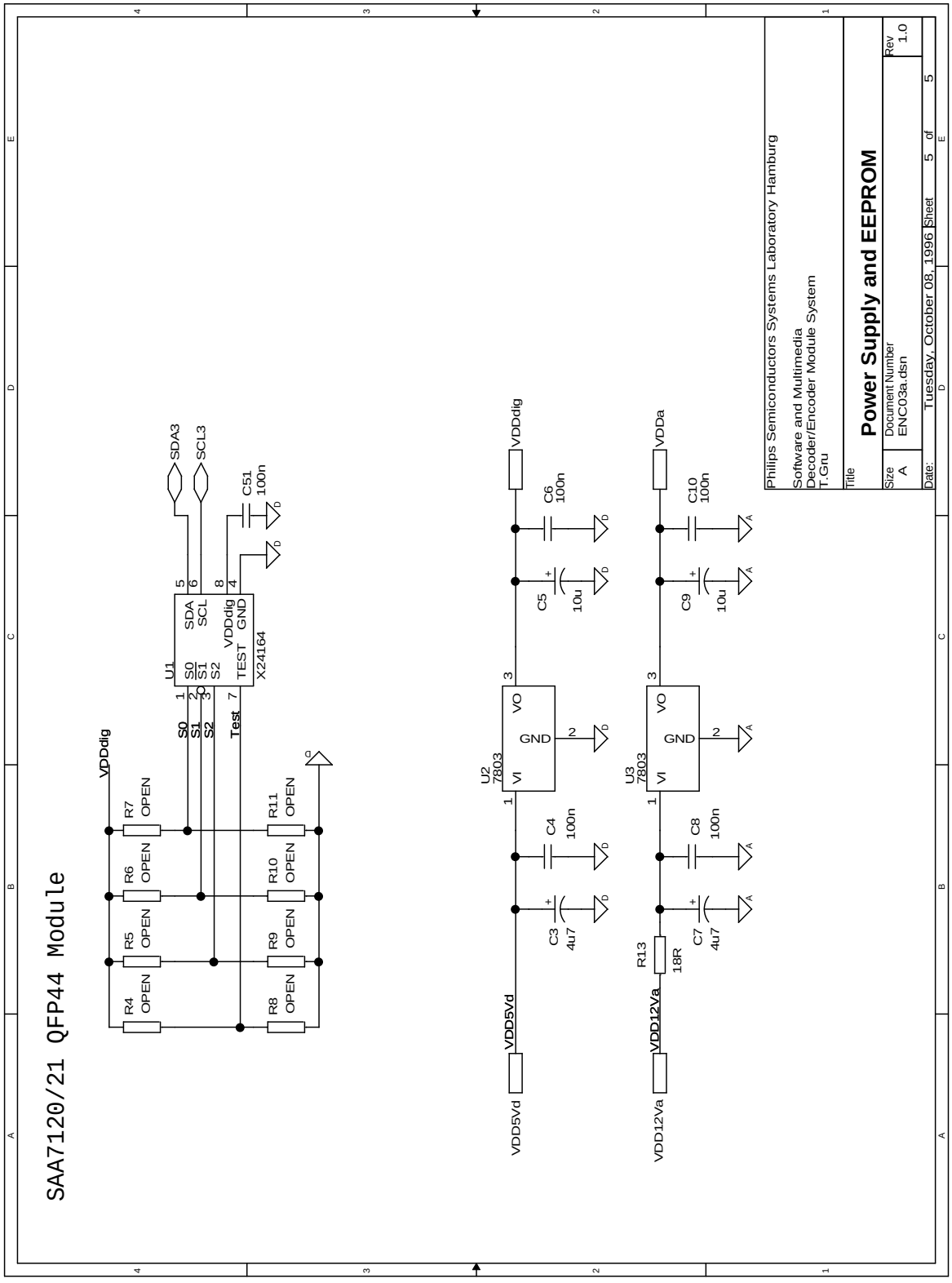
11.1.3 Inputs of ENCMOD03



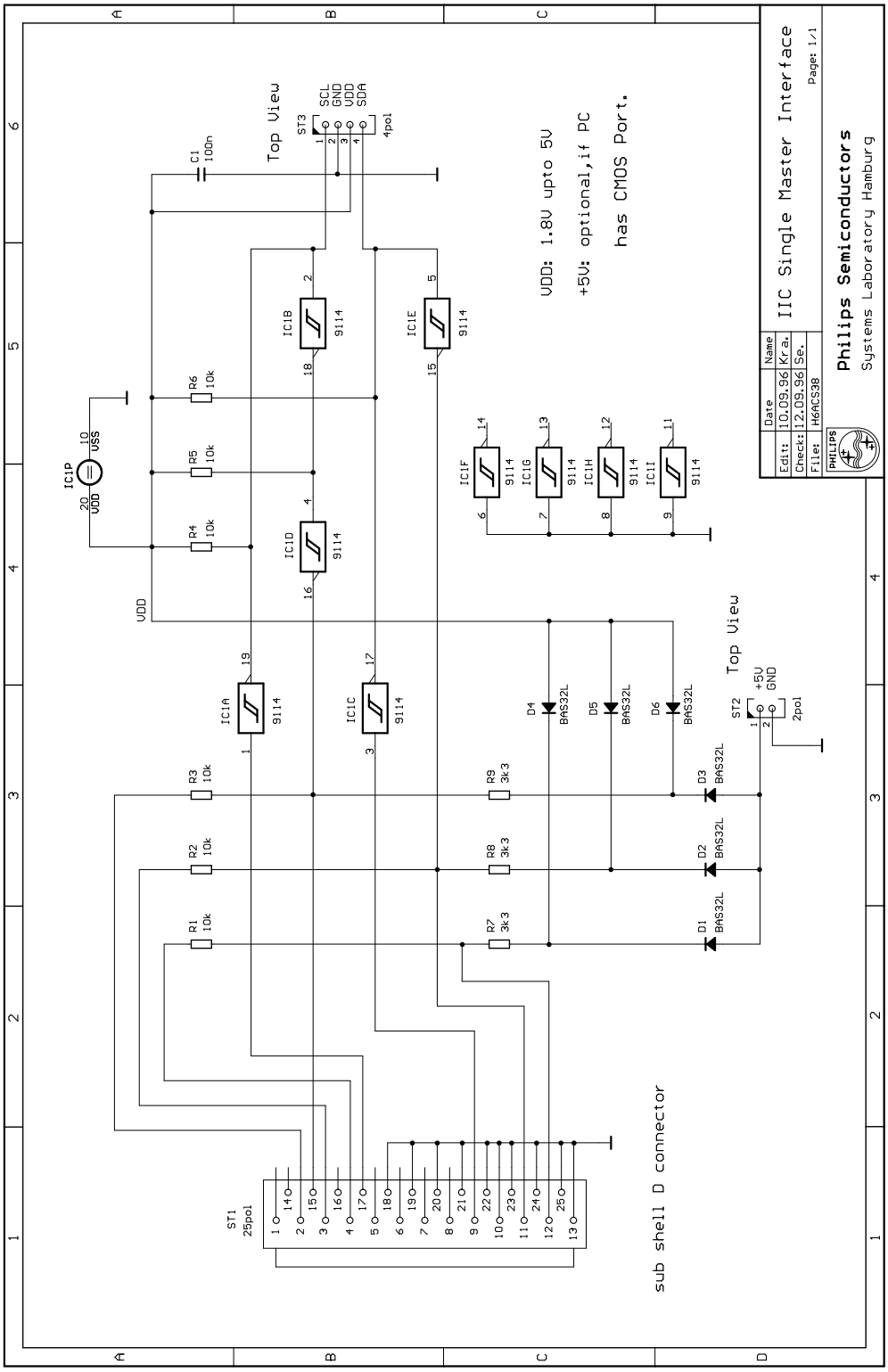
11.1.4 Outputs of ENCMOD03



11.1.5 Power Supply and EEPROM of ENCMOD03

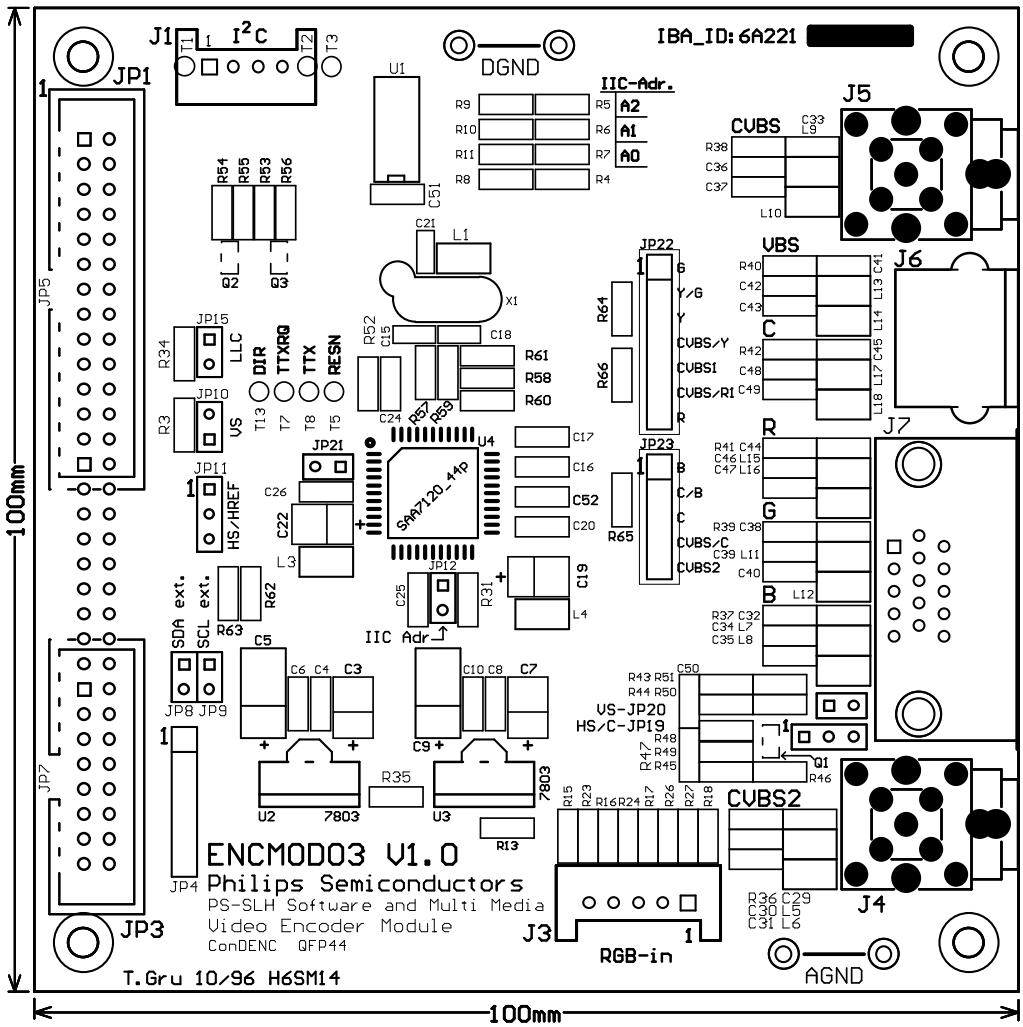


11.1.6 I²C Interface H6ACS38

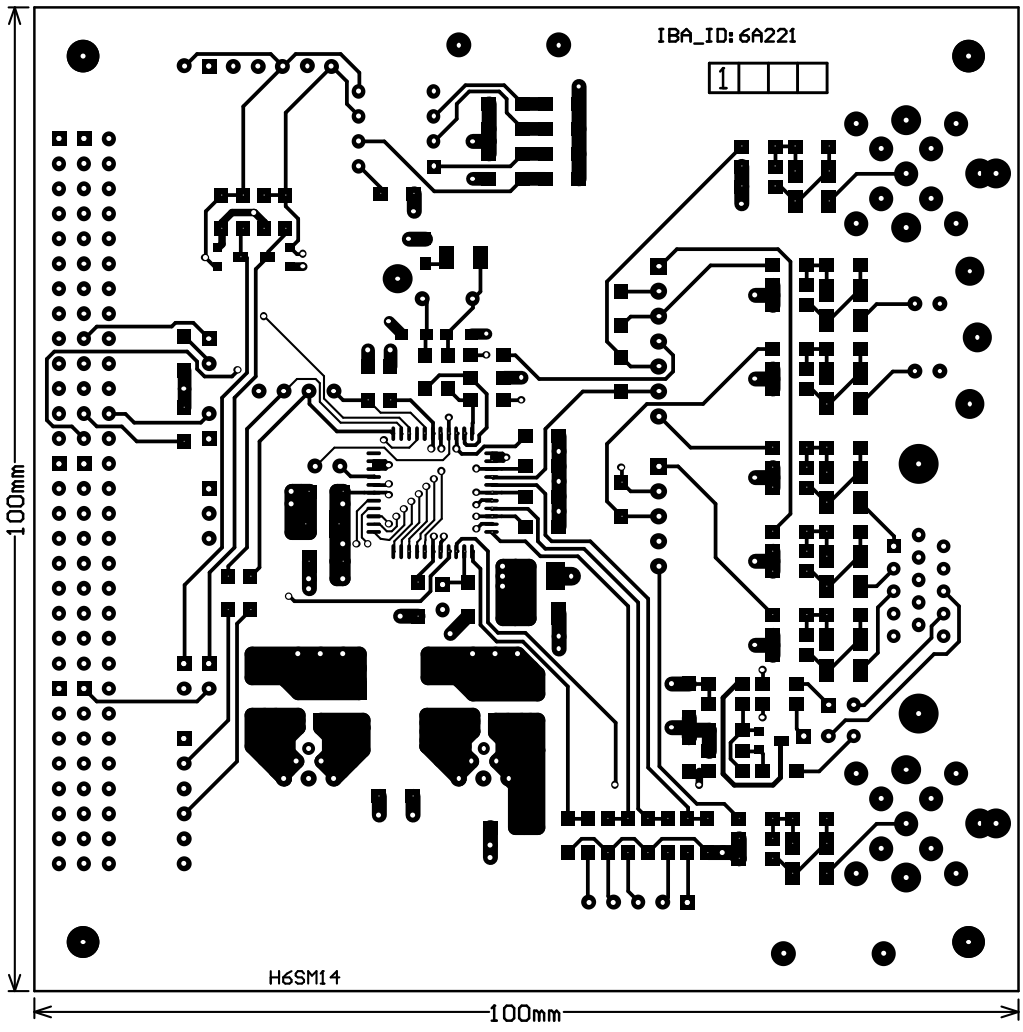


11.2 Layout

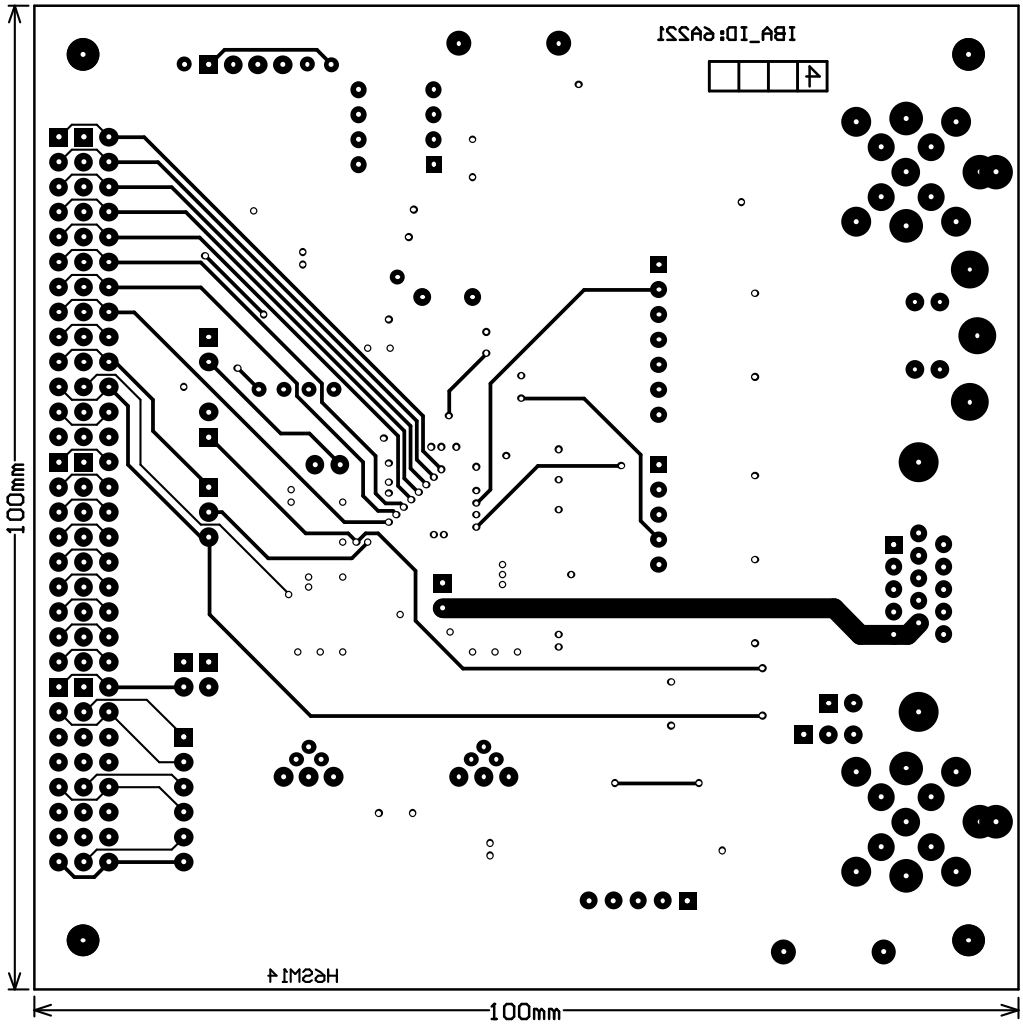
11.2.1 Top placement of ENCMOD03



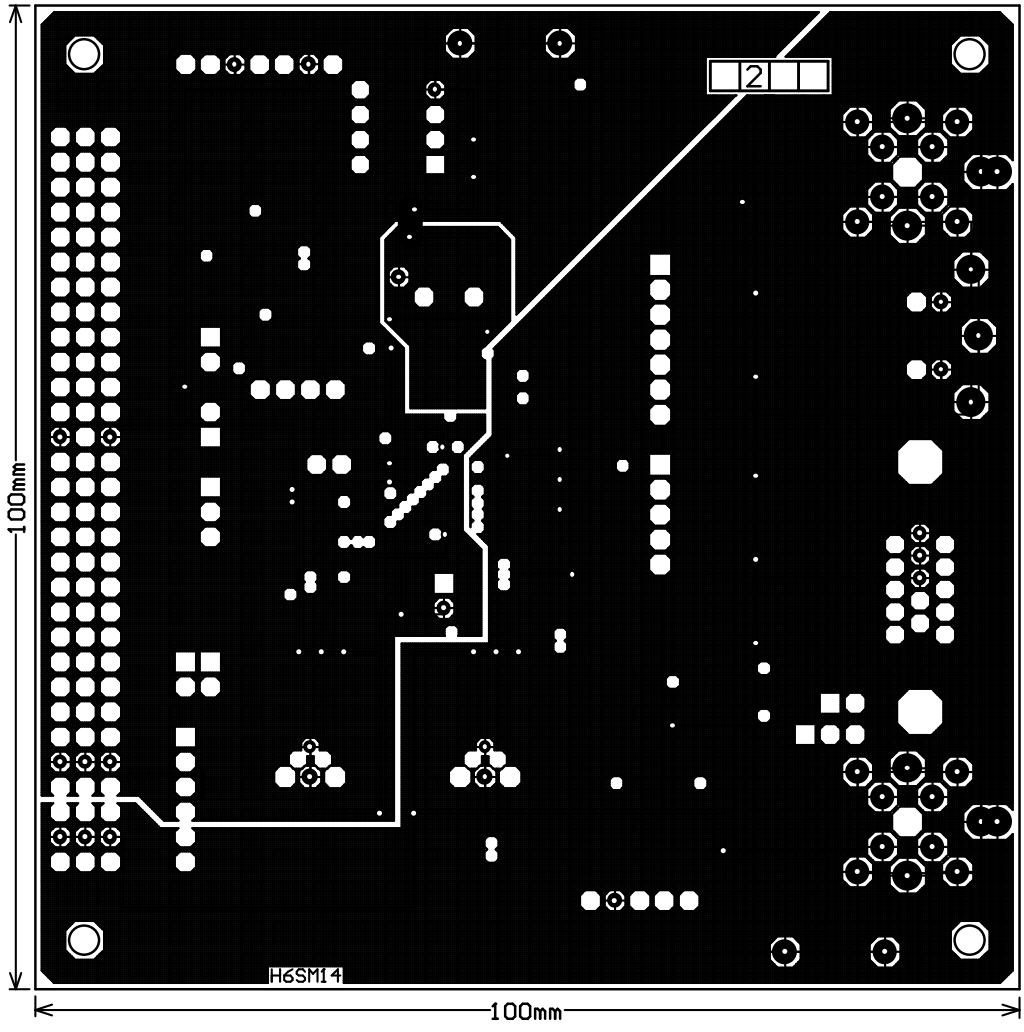
11.2.2 Routing of top layer of ENCMOD03



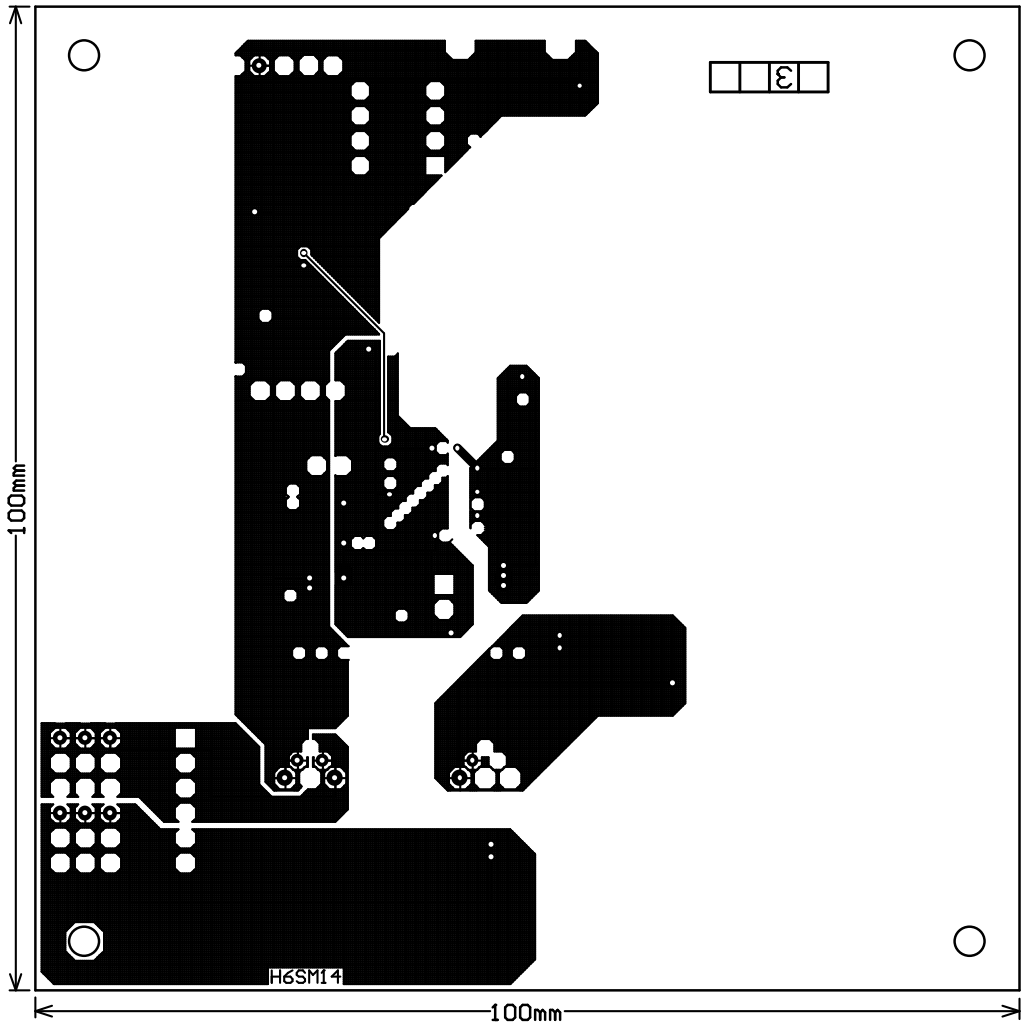
11.2.3 Routing of bottom layer of ENCMOD03



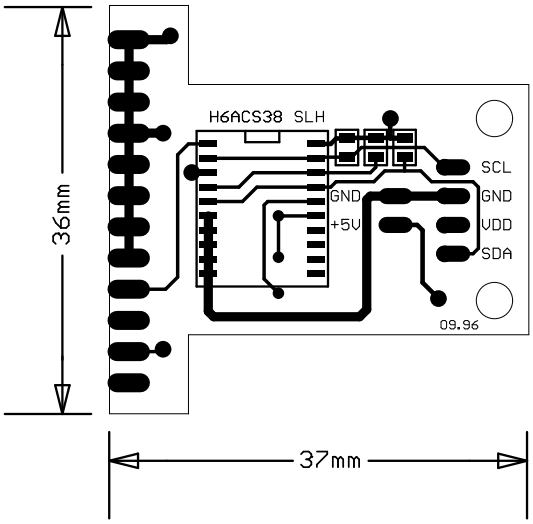
11.2.4 Routing of ground plane layer of ENCMOD03



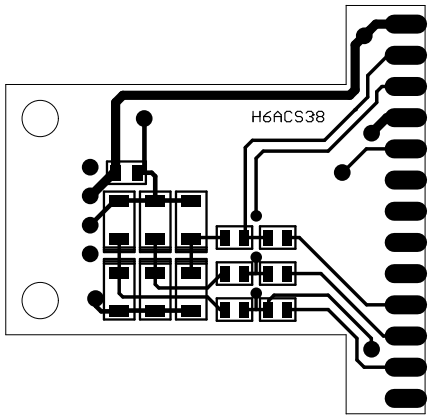
11.2.5 Routing of power supply layer of ENCMOD03



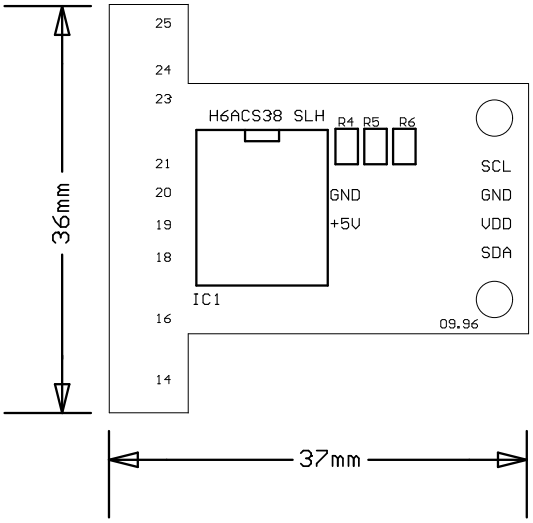
11.2.6 Routing and Placement of I²C Interface H6ACS38



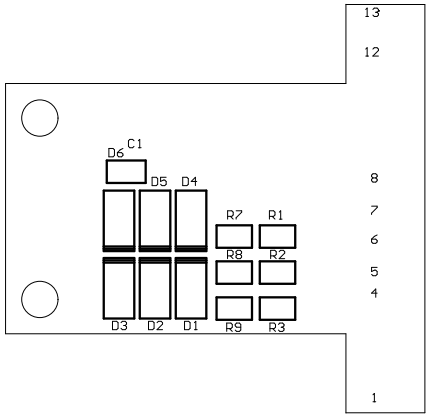
Top routing



Bottom routing



Top placement



Bottom placement